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(56) Documents cited
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(58) Field of search
UK CL (Edition J) H1R RAC RAL RAN RAP RBD
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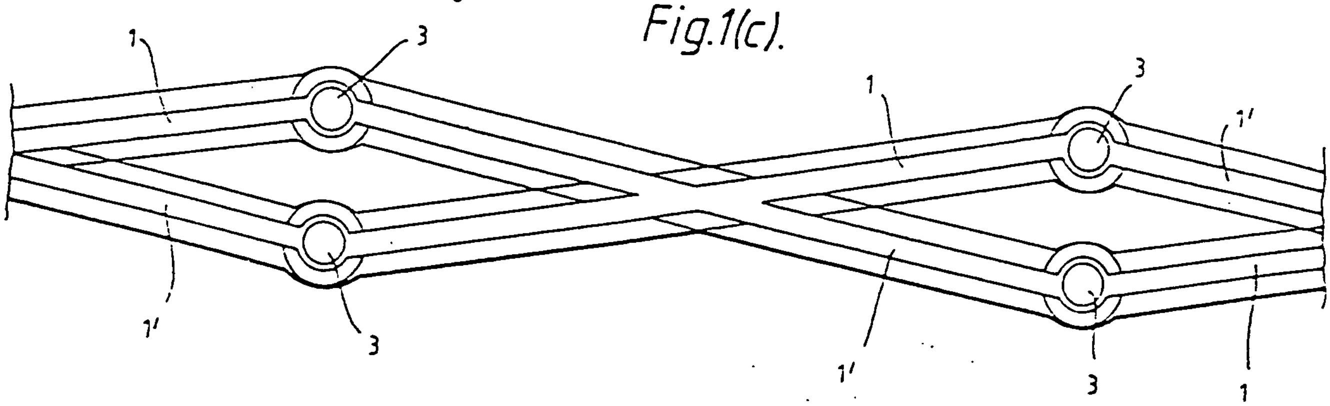
(54) Conductive track arrangement on a printed circuit board

(57) A printed circuit board includes conductive tracks that alternate between two layers and repeatedly cross one another in a manner to simulate conventional twisted wirings. The tracks are formed by interconnecting individual segments 1, 1' formed on the two layers by vias 3. The layers may be provided with conductive areas to provide shielding, and further shielding layers may also be added. The resulting PCB may be of a large-scale type that can be used to replace conventional twisted and shielded wiring.

Fig.1(c).



At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy

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Fig.1(a).

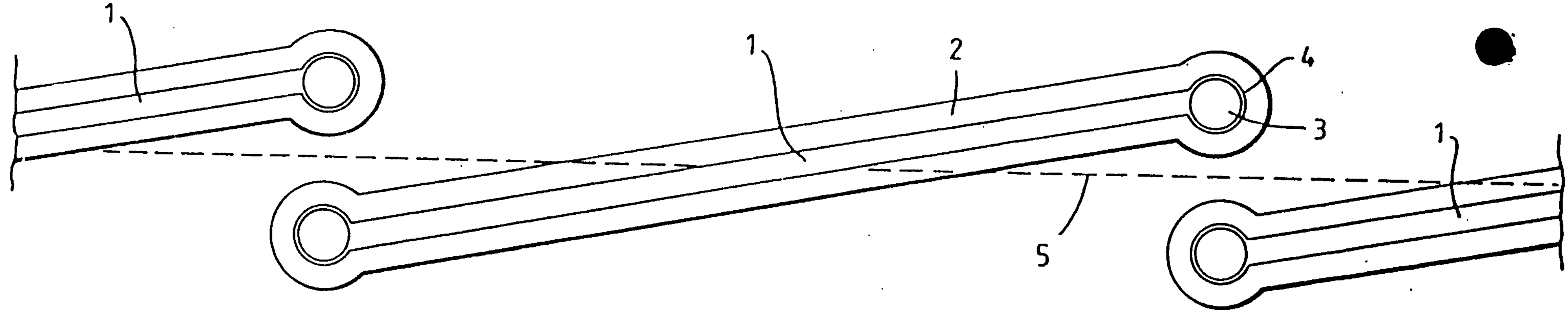
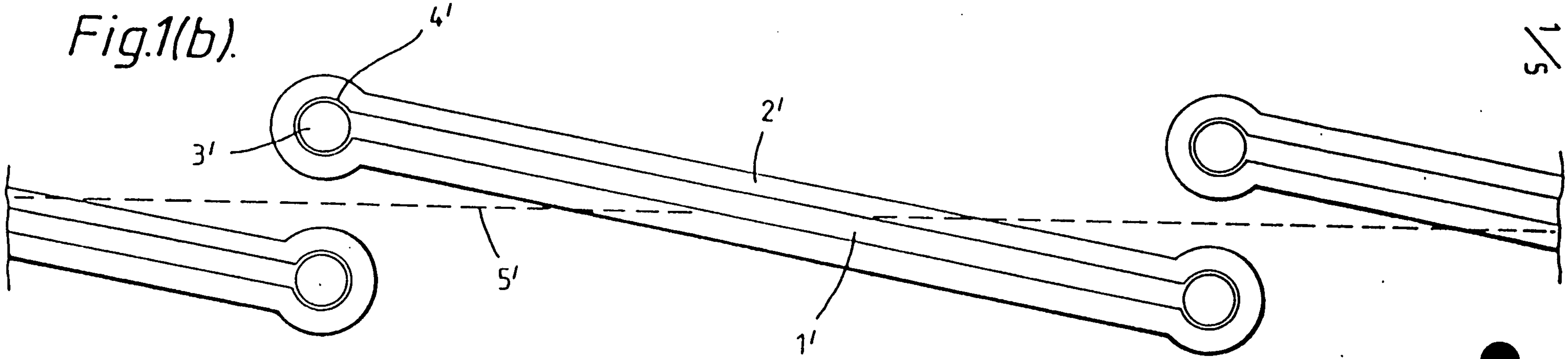


Fig.1(b).



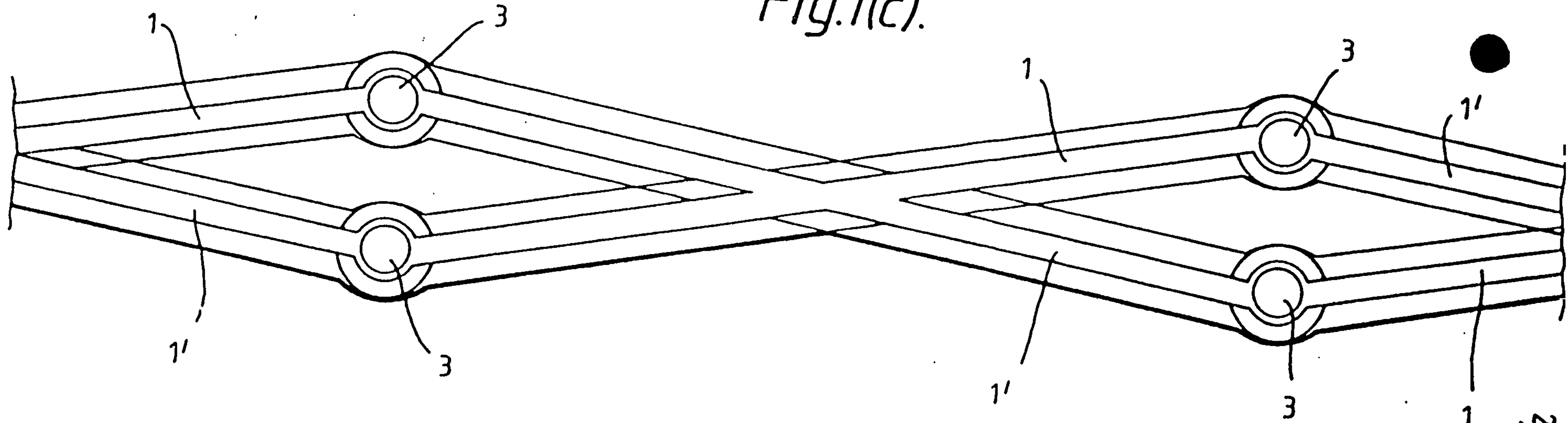


Fig.1(c).

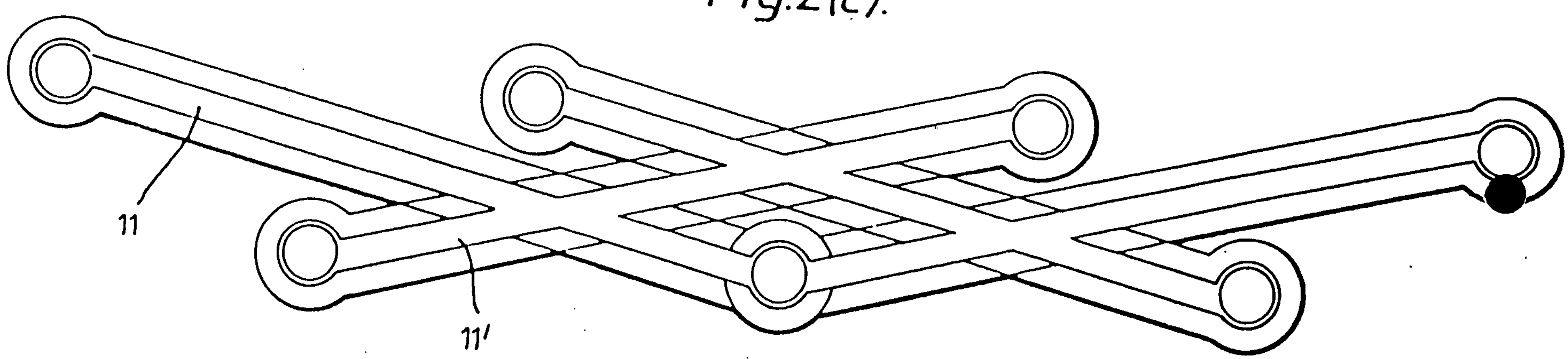


Fig.2(c).

Fig.2(a).

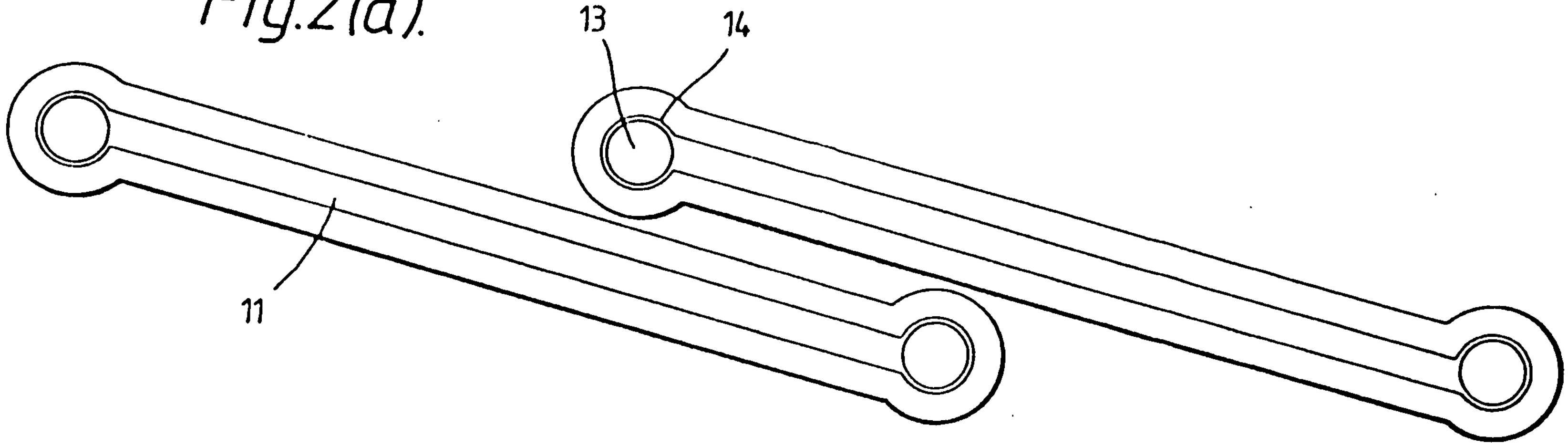


Fig.2(b).

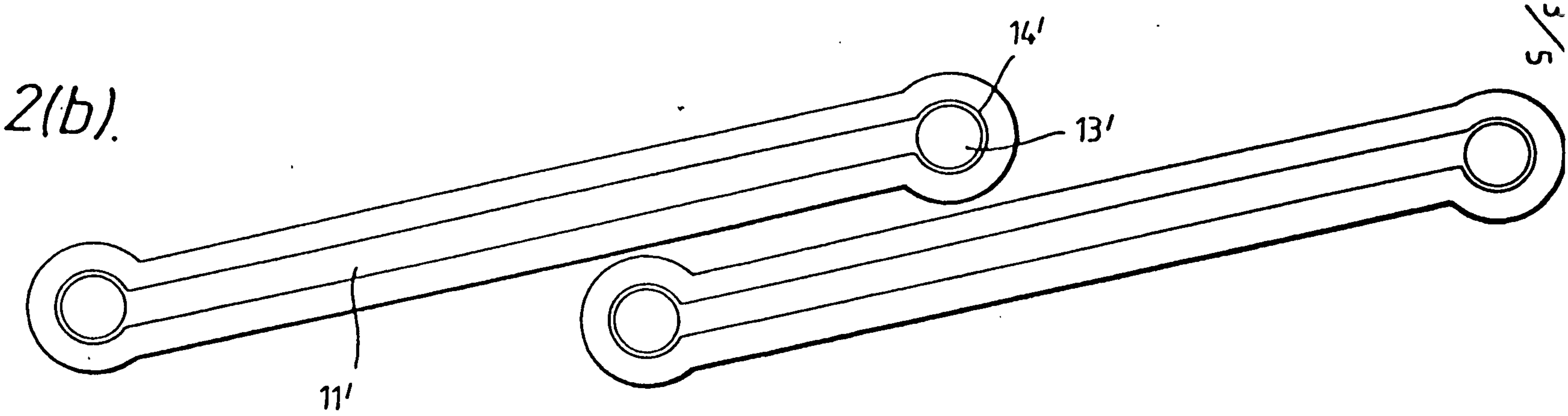


Fig.3(a).

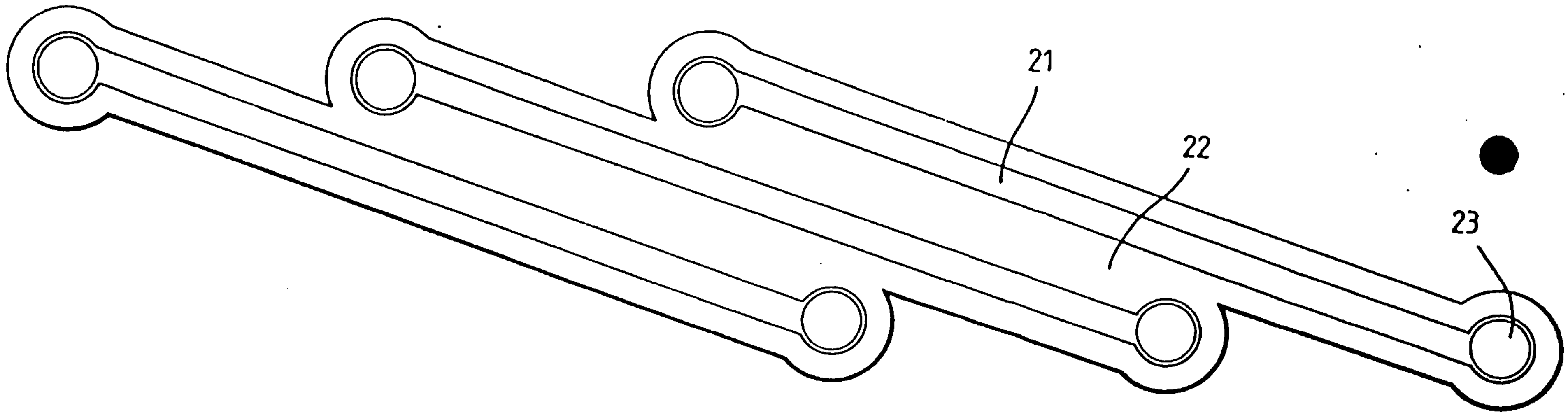


Fig.3(b).

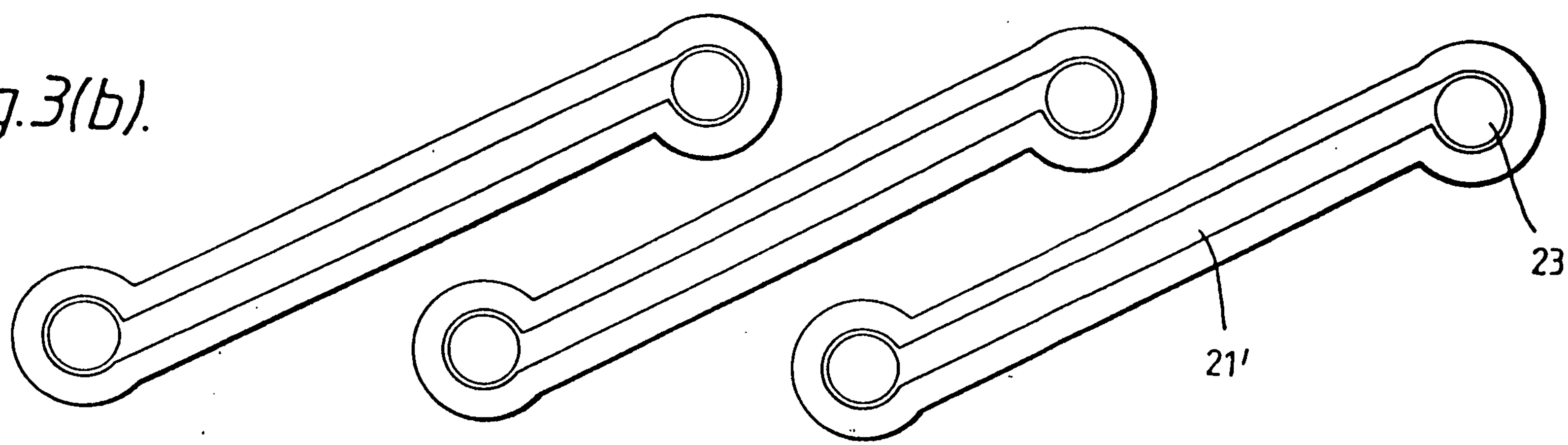
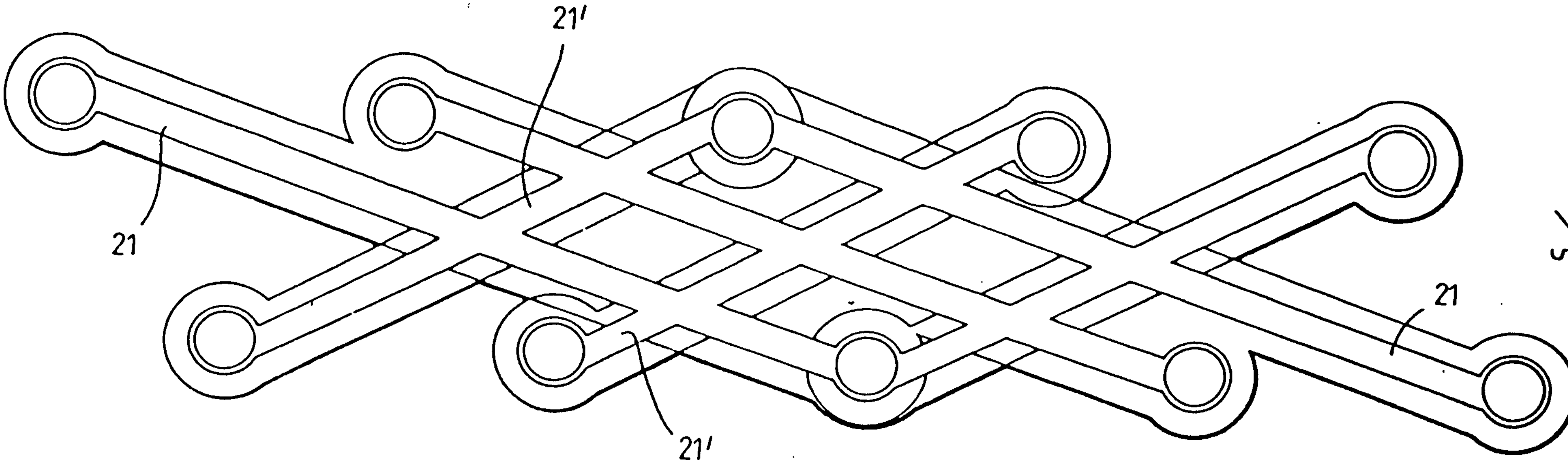


Fig.3(c).



PRINTED CIRCUIT BOARD

This invention relates to a printed circuit board (PCB), and in particular to a large-scale PCB that may be used to replace conventional wiring arrangements in, for example, an aircraft.

Conventional wiring in an aircraft, such as that interconnecting avionics units for example, generally consists of bundles of a number of individual wires. Such bundles are, however, disadvantageous in that they are large and heavy, and furthermore can make it difficult to identify a particular wire when, for example, fault checking. For such reasons it would be desirable to replace such wiring with a large-scale PCB, having dimensions of up to about 1m. Individual wires could then be replaced by conductive tracks on the PCB. A problem with this however is that conventional wiring is provided with means of shielding the wiring from unwanted electromagnetic-interference. Such interference may be created by sources external of the wiring, or may be generated by currents flowing in the wiring. Individual wires may be regarded as 'emissive', indicating that they generate such interference, or 'susceptible', indicating that they are particularly vulnerable to such interference.

Conventional ways of mitigating problems with such interference includes providing copper shielding, and twisting wires together. In the past it has been difficult

to provide corresponding shielding to wires formed as tracks on a PCB.

According to the present invention there is provided a printed circuit board comprising two layers, each said layer including a linear series of individual conductive track segments, said series being generally superimposed on each other and extending in the same direction, means being provided at the ends of each segment to connect a said segment in one layer to a said segment in the other layer.

By means of this arrangement is is possible to construct conductive tracks, by connecting segments from both layers, that 'interweave' and overly each other in a manner to simulate the twisting of conventional wiring.

In a particularly preferred arrangement the track segments in each said layer are disposed at an angle to the direction of the series, the segments in one layer being angled in the opposite sense to those in the other layer. By 'angled in the opposite sense' it is meant that if, say, the segments cross an imaginary line extending in the direction of that series from left to right, the other series of segments will cross the line from right to left.

In one embodiment alternate segments in one layer are interconnected by a segment in the other layer. This arrangement provides two tracks simulating a two-core twist.

In another embodiment every third segment in one layer is interconnected with a segment from the other layer. This

provides three tracks simulating a three-core twist. Naturally this process can be extended; for example every fourth segment being interconnected to define four tracks, simulating a conventional wire of a four-core twist.

Preferably the interconnection between two track segments is by means of a via comprising a bore extending between said layers normal to the plane of the printed circuit board, the interior surface of the bore being provided with a conductive coating.

Such an arrangement allows tracks to be defined that simulate conventional twisted wires and provide similar shielding. It is preferred however to provide the PCB with further shielding in the form of one or more areas of conductive materials (eg copper) on the regions of said layers not defining said track segments, and/or such areas formed on further layers of said PCB. Such areas may be substantially uninterrupted, or may comprise complementary areas formed on adjacent layers. Where such areas are formed on layers not defining tracks, the areas may extend over the whole layer, or only that region overlying the tracks defined on other layers.

Some embodiments of the invention will now be described by way of example and with reference to the accompanying drawings, in which:-

Figures 1(a) and (b) each show a part of a track segment series formed on a layer, with Figure 1(c) showing

the segments of Figures (a) and (b) superimposed and interconnected to form two tracks,

Figures 2(a), (b) and (c) are views similar to Figure 1 but showing a three track arrangement,

Figures 3(a), (b) and (c) are similar to Figures 1 and 2, but showing a four track arrangement.

Referring firstly to Figure 1(a) there is shown a part of a series of conductive track segments 1 formed on a PCB substrate layer formed of, eg, epoxy glass. Such segments may be formed by conventional techniques, such as by removing (for example by etching) the areas 2 surrounding the segments from a substrate layer covered in copper. At the ends of each segment 1 are formed vias 3 by means of which the segments 1 may be connected to corresponding segments formed on an adjacent layer. Each via 3 consists of a hole extending through the layer generally at right-angles to the surface of the layer, the interior surface of the hole being provided with a conductive coating 4.

The segments 1 of Figure 1(a) are arranged generally in a line extending from left to right in the Figure. Each individual segment 1 is however disposed at an angle to that line, as illustrated by imaginary centre line 5. Each segment 1 is of such a length and at such an angle that the ends of successive segments 1 lie generally adjacent on either side of the imaginary centre line 5.

The series of conductive track segments shown in Figure 1(b) is identical to that of Figure 1, except that the segments 1' are angled in the opposite sense to those of Figure 1(a), that is to say they cross the centre line 5' in the opposite direction. In all other respects, eg, the angle presented to the centre line, the length of each segment and the spacing of the segments in the series, the series shown in Figure 1(b) is substantially identical to that of Figure 1(a).

The series of Figures 1(a) and 1(b) are formed on separate layers of a PCB. In the PCB the series are superimposed, and Figure 1(c) shows the result of this superimposition. From Figure 1(c) it will be clearly seen, that when superimposed an individual segment in one series is connected at each end to alternate segments from the other series, thus defining two separate conductive tracks. Looking at Figure 1(c) one track includes segment 1 connected at each end to respective segments 1' by means of vias 3. The other track includes a segment 1' connected at each end to segments 1. If one assumes that the series of Figure 1(a) is superimposed on that of Figure 1(b), each segment 1 will lie over its corresponding segment 1'. Since each track is defined by alternating segments 1 and 1', each track will alternately go over and then under the other track. In this way the two conductive tracks effectively simulate a conventional two-core twisted wire.

It will of course be appreciated that Figures 1(a), (b) and (c) show only a part of a series of track segments 1, 1' and that the series could be extended to any desired length.

The precise dimensions of the 'twist' may be selected as appropriate for any particular application. However, as an example, the overall pitch of the twist may be 1" (25.4mm), ie the length over which one track will cross its partner twice (the second crossover occurring after transfer to the alternate layer by means of the vias) and then return to the start point of the subsequent twist. Each segment may have a width of 0.015" (0.381 mm) and the gap 2 defining the track is preferably 0.01" (0.254 mm) wide. Each via has a diameter of about 0.040" (1.016 mm).

The width of each series of track segments 1, 1' and thus of the resulting tracks, is such that the tracks lie within a track envelope 0.2" (5.08 mm) wide. The area of this envelope, on both layers, outside of the track defining gaps 2, 2' is conductive (eg copper) to provide close proximity shielding for the tracks.

Figures 2(a) and 2(b) show parts of series of track segments 11, 11' formed on alternate layers of a PCB, that when superimposed as shown in Figure 2(c) may be interconnected to define three "twisted" tracks. As with the two-core twist embodiment of Figure 1, an individual track segment 11 of one series is connected at each end by vias 13 to respective segments 11' of the other series.

However, instead of being connected to alternate segments, as in Figure 1, the segments 11 are connected to every third segment 11'. That is to say each segment 11 is connected to two segments 11', these two segments 11' being spaced by two other segments 11'. Repeating this sequence along the two series of segments 11, 11' results in three conductive tracks being formed, with each track switching from one layer of the PCB to the other at the interconnections between segments at vias 13. As the tracks switch from one layer to the other they repeatedly pass over and under each other in the manner of conventional three-core twisted wiring.

The tracks of Figure 2(c) are kept within the same overall track envelope on the tracks of Figure 1(c). To achieve this the track segments 11, 11' are shorter, more closely spaced and more sharply angled then those of Figures 1(a)-(c).

Figures 3(a)-(c) show a further embodiment in which four tracks are defined to simulate four-core twisted wiring. As before one track segment 21 in one layer is connected between two segments 21' in the other layer. In this embodiment however every fourth segment 21' are connected by one segment 21, that is to say between each pair of segments 21' are three further segments 21' which are, of course, connected in turn to their own respective segments 21. As before, this procedure is continued and

defines four separate tracks alternating between layers and criss-crossing as in the other embodiments.

This embodiment does, however, differ in certain other respects from those shown in Figures 1(a)-(c) and 2(a)-(c). Firstly, in order to maintain the overall track width within the same 0.2" envelope, the segments 21' in one layer must be shorter than the segments 21 in the other layer. The shorter segments may be located in either the upper or lower layer as desired. Related to this is the further difference that the longer segments 21 are spaced so close together that the track segment defining gaps 22 merge together between segments.

In the embodiments of Figures 2(a)-(c) and 3(a)-(c) the remainder of the track envelope beyond the track segment defining gaps 12, 22 may be conductive to provide close proximity shielding for the 'twisted' tracks.

The present invention may be employed in the construction of large-scale PCBs replacing conventional wiring. Such a PCB may comprise several layers, certain layers defining 'twisted' tracks as discussed above, others providing further shielding in addition to the close proximity shielding described above. Such additional shielding may be provided by layers having large conductive (eg, copper) areas extending either over substantially the entire area of the PCB, or at least those regions in which there are formed tracks. Shielding may also be provided by

adjacent layers having complementary conductive areas, for example complementary hatched areas. In all these cases it may be desirable to interconnect the various shielding conductive areas, and this may be achieved by means of vias similar to those interconnecting the track segments.

One possible, and advantageous, structure for the PCB would be to form the emissive and susceptible tracks on different pairs of layers and separate these tracks from each other by means of intermediate shielding layers. If this is not possible and emissive and susceptible tracks must be formed on the same pair of adjacent layers, they can at least be horizontally separated in the layers.

CLAIMS

1 A printed circuit board comprising two layers, each said layer including a linear series of individual conductive track segments, said series being generally superimposed on each other and extending in the same direction, means being provided at the ends of each segment to connect a said segment in one layer to a said segment in the other layer.

2 A printed circuit board according to Claim 1 wherein the track segments in each said layer are disposed at an angle to the direction of the series, the segments in one layer being angled in the opposite sense to those in the other layer.

3 A printed circuit board according to Claim 1 or 2 wherein alternate segments in one layer are interconnected by a segment in the other layer.

4 A printed circuit board according to Claim 1 or 2 wherein every third segment in one layer are interconnected by a segment in the other layer.

5 A printed circuit board according to Claim 1 or 2 wherein every fourth segment in one layer are interconnected by a segment in the other layer.

6 A printed circuit board according to any preceding claim wherein said layers further include conductive areas to provide shielding.

7 A printed circuit board according to any preceding claim including further layers bearing conductive shielding areas.

8 A printed circuit board according to Claim 6 or 7 wherein at least some of said conductive areas are interconnected.

9 A printed circuit board according to any preceding claim wherein interconnections between layers are by means of vias.

10 A printed circuit board substantially as hereinbefore described with reference to the accompanying drawings.

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